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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/614,154	07/11/2000	Martin J. Edwards	PHB 34,365	1602

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EXAMINER	
SHAPIRO, LEONID	
ART UNIT	**PAPER NUMBER**
2673	16

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/614,154	EDWARDS, MARTIN J.	
	Examiner	Art Unit	
	Leonid Shapiro	2673	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 January 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *9-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *9-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

1. Claim 13 is rejected under 35 U.S.C. 102(e) as being anticipated by Matsueda et al. (US Patent 6,384,806 B1).

Matsueda et al. teaches an active matrix array device (See Col. 1, Lines 8-12) comprising: substrate (See Fig. 15, item 100, Col. 19, lines 44-45); an array of individually addressable matrix elements carried on substrate (See Fig. 1, item 40), a set of address conductors connected to array of matrix elements and carried on substrate (See Fig. 15, item 41), set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 15-17, items 10, 100, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58) and an addressing circuit including a multiplexing circuit (inside of 200A and 200B, Fig. 17) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines , multiplexing circuit being arrange to couple sequentially each group of set of address conductors to plurality of signal lines with each address conductor in a group being coupled to a respective one of signal bus lines (inside of 200A and 200B, Fig. 17) and a plurality of signal processing circuits (digital drive circuit 200 of Fig. 15) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 15-17, items 10, 100, 101, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and

Col.19, lines 13-58), wherein an order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-45). Notice that D/A converters on both sides of LCD panel.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 9-10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda et al. in view of Enami et al. (US Patent no. 5,892,493).

As to claim 9, Matsueda et al. teaches an active matrix array device (See Col. 1, Lines 8-12) comprising: substrate (See Fig. 15, item 100, Col. 19, lines 44-45); an array of individually addressable matrix elements carried on substrate (See Fig. 1, item 40), a set of address conductors connected to array of matrix elements and carried on substrate (See Fig. 15, item 41), set of address conductors being arranged in a series of groups with each group including successive address conductors (See Fig. 15-17, items 10, 100, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58) and an addressing circuit including a multiplexing circuit (inside of 200A and 200B, Fig. 17) integrated on substrate and connected to set of conductors, multiplexing circuit having a plurality of signal bus lines , multiplexing circuit being arrange to couple sequentially each group of set of address conductors to plurality of signal lines

with each address conductor in a group being coupled to a respective one of signal bus lines (inside of 200A and 200B, Fig. 17) and a plurality of signal processing circuits (digital drive circuit 200 of Fig. 15) integrated on substrate, each signal processing circuit connected to a respective bus line (See Fig. 15-17, items 10, 100, 101, 200, 41, 42, 30, in description See Col.20, Lines 30-64 and Col.19, lines 13-58).

Matsueda et al. does not show a first signal processing circuit associated with a first address conductor of a first group of address conductor and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on substrate.

Enami et al. teaches a first signal processing circuit (inside of multiplexer 38 and data line driver 40 in Fig. 1) associated with a first address conductor (d1B in Fig. 1) of a first group of address conductor (d1B-dnB in Fig. 1) and a second signal processing circuit (inside of multiplexer 38 and data line driver 40 in Fig. 1) associated with a last address conductor (dnA in Fig.1) of a second group of address conductors (d1A-dnA in Fig.1) are adjacent on substrate (See Col. 7, Lines 46-61).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement a first signal processing circuit associated with a first address conductor of a first group of address conductor and a second signal processing circuit associated with a last address conductor of a second group of address conductors are adjacent on substrate as shown by Enami et al. in the Matsueda et al. apparatus in order to selectively connect the driver to any one of sets data line groups (See Col. 2, Lines 8-15 in the Enami et al. reference).

As to claim 10, Matsueda et al. teaches signal processing circuits are arranged in series in a line parallel to multiplexing circuit (See Figs. 15-17, items 200, 101A, 101B, 200A, 200B, in description See Col. 19, Lines 28-34 and Col.20, Lines 29-48). Notice that multiplexing circuits are in the shift registers on both sides of LCD panel.

As to claim 12, Matsueda et al. teaches an active matrix array device with order in which processing circuit blocks are arranged physically on the device substrate is different to the physical order of the signal bus lines to which they are respectively connected (See Fig. 17, items 200A, 200B, in description See Col.20, Lines 29-45). Notice that D/A converters on both sides of LCD panel.

3. Claim 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsueda et al. and Enami et al. in view of Yamazaki et al. (US Patent 6, 144,426).

As to claim 11, Matsueda et al. and Enami et al. do not show a first subset of signal processing circuits are arranged in a first row and a second subset of signal processing circuits are arranged in a second row and offset from the first row in a brick-like fashion.

Yamazaki et al. teaches place microlens array in brick fashion (arranged like laid bricks) (See Fig. 3, item 105, in description see Col. 8, Lines 9-18).

It would have been obvious to one of ordinary skill in the art at the time of invention to implement layout of signal processing circuits in a brick-like fashion as shown by Yamazaki et al. in the Matsueda et al. and Enami et al. apparatus in order to selectively connect the driver to any one of sets data line groups (See Col. 2, Lines 8-15 in the Enami et al. reference).

Response to Arguments

4. Applicant's arguments filed on 01-30-04 have been fully considered but they are not persuasive:

On pages 6-8 Applicant agreed that Enami et al. reference satisfied all limitations of, except eighth, the final limitation of independent claim 9.

On page 8, 3rd paragraph Applicant stated that limitation is not by Enami et al. However, Enami et al. teaches a first signal processing circuit (inside of multiplexer 38 and data line driver 40 in Fig. 1) associated with a first address conductor (d1B in Fig. 1) of a first group of address conductor (d1B-dnB in Fig. 1) and a second signal processing circuit (inside of multiplexer 38 and data line driver 40 in Fig. 1) associated with a last address conductor (dnA in Fig.1) of a second group of address conductors (d1A-dnA in Fig.1) are adjacent on substrate (See Col. 7, Lines 46-61).

On same page, last paragraph Applicant stated, that Enami et al. teaching is identical to the prior art illustrated in Fig. 3. However, Examiner will direct Applicant to look to the 2nd page, last paragraph Applicant's Remarks dated 06.10.03 in response to 112, 1ST paragraph rejection of claim 9. The applicant stated, that last limitation of claim 9, as illustrated in Fig. 2, is enabled by the description of signal processing circuit being associated with the first conductor C10, of group G2 due to the coupling of bus line to address conductor C10, signal processing circuit being associated with the last address conductor C9 of group G1 due to the coupling of bus line to conductor C9, and signal processing circuits being adjacent on substrate. This is the same situation as Fig. 1 of Enami et al. reference with only difference that groups called A and B

instead of G1 and G2. Therefore the last limitation of claim 9 is satisfied by the Enami et al. reference.

Conclusion

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Telephone inquire

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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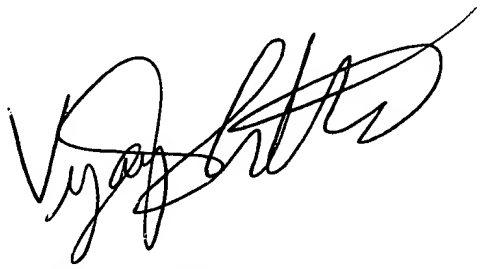

VIJAY SHANKAR
PRIMARY EXAMINER